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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,788	01/22/2004	Samir Chaudhry	CHAUDHRY	6125

47396 7590 01/04/2006

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EXAMINER	
PHAM, LONG	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 01/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/762,788	CHAUDHRY ET AL.	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23,24,26-32 and 41-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *23,24,26-32 and 41-46* is/are allowed.

6)☒ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/21/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The incorporation of essential material in the specification by reference to an unpublished U.S. application, foreign application or patent, or to a publication is improper. Applicant is required to amend the disclosure to include the material incorporated by reference, if the material is relied upon to overcome any objection, rejection, or other requirement imposed by the Office. The amendment must be accompanied by a statement executed by the applicant, or a practitioner representing the applicant, stating that the material being inserted is the material previously incorporated by reference and that the amendment contains no new matter. 37 CFR 1.57(f).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent

either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 23, 24, 26-32, and 41-46 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-10 of U.S. Patent No. 6,551,946 in view of Holloway et al. (US patent 4,845,047), Adan (US patent 6,288,425), and Ueno et al. (US patent 6,815,295). Claims 1-10 of US Patent No. 6,551,946 teach the invention as recited in present claims 23 and 41-46.

With respect to claim 23, claims 1-10 of US Patent No. 6,551,946 fail to teach forming within the substrate a source, a drain, and a channel extending from the source to the drain, wherein the source and the drain do not include a lightly doped region and forming a gate structure over the substrate, the gate structure having a length of approximately 1.25 micrometers or less and being coextensive with a width of the oxide.

Holloway et al. teach a process for fabricating an integrated circuit, comprising (see fig. 1 and col. 6, lines 45-55):
providing a doped substrate having a source, a drain, and a channel extending from said source to said drain, wherein said source and said drain do not include a lightly doped regions;
forming an oxide over said channel, said oxide being defined by a width, wherein said oxide and said substrate forms an interface that is substantially planar; and forming a gate structure over a substrate, said gate slructure having a length of approximately 1.25 micrometer and being coexlensive with said width of said oxide. See fig. 1 and col. 6, lines 45-55.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the above teaching of Holloway et al. into the device of claims 1-10 of US Patent No. 6,551,946 to allow formation of MOS device integrated circuit.

With respect to claim 24, Holloway et al. fail to teach that the channel is formed before the source and drain are formed.

Adan teaches a process in which channel region is formed before source and drain are formed. See col. 2, lines 50-65.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate Adan's above teaching into the process of Holloway et al. to improve manufacturing yield. See col. 8, lines 40-45.

With respect to claim 26, Holloway et al. fail to teach that the channel is doped by a halo implantation.

However, doping channel by halo implantation is well-known in the art.

With respect to claim 27, Holloway et al. fail to teach that the gate length is in the range between .05 to .25 micrometer.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to reduce the length of gate because it is known that shorter gate length would achieve device scaling.

With respect to claim 28, Holloway et al. fail to teach gate oxide comprises of a first oxide layer and a second oxide layer.

Ueno et al. teach a process in which a gate oxide comprises of a first oxide layer and a second oxide layer. See col. 28, lines 1 5-25.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to form gate oxide made from a first oxide layer and a second oxide layer to reduce the processing steps. See col. 28, line 38.

With respect to claim 29, Holloway et al. teach a spacer formed adjacent the gate structure.

However, An omission of an element and its function if the function of the element is not desired is obvious. See Ex parte Wu , 10 USPQ 2031 (Bd. Pat. App. & Inter. 1989).

With respect to claim 30, Holloway et al. fail to teach the range for the thickness of gate oxide layer.

However, il would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value or range for the thickness of gate oxide layer through routine experimentation and optimization to obtain optimal or desired device performance because it is a result-effective variable and there is no evidence indicating that it is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

With respect to claims 31 and 32, Holloway et al. fail to teach the ranges for the concentration of lhe source, drain, and channel.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value or range for the concentration of the source, drain, and channel through routine.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Pham
Primary Examiner
Art Unit 2814

LP